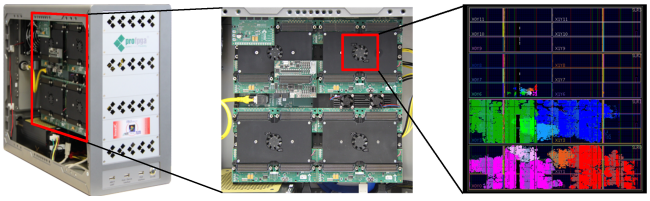
Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Assistant (Student)

Frequency Optimization of a FPGA Prototype



Description

Our NoC-based many-core design is implemented on multiple Xilinx Virtex7 FPGAs. It is currently frequency limited by individual components.

Goal

The goal of this work is to optimize the overall frequency of an FPGA design.

This work includes:

- Indetification of the critical paths of the design
- Pipelining the design to reach higher frequencies

Prerequisites

For this challenging task, several prerequisites should be met:

- Very good knowledge of VHDL
- Very good knowledge of the Xilinx Vivado Synthesis Tool
- Very good experience with FPGA design
- Very good knowledge about digital circuit design

Application

If you are interested, send me an email with your CV, your transcript of records and summary of your experience attachted.

Contact

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Advisors