

Master's Thesis

# **Simulator Support for Dynamic Data Migration**

## **Description**

Hitting a wall is not a pleasant thing. Computer systems to compute the last decades. Being able to break the memory wall in the mid 90's and the power wall in 2004, it now faces the next crucial barrier for scalabilty. Although being able to scale systems to 100's or 100's or 100's or through NoCs, performance doesn't scale due to data-to asked librarier. Not now face the locality wall.

The newest trend to tackle this issue is data-task migrat

# Router Router Processing No. 24 Memory No. 2

CPU CPU

-Core CPU

or near memory.

CPU

CPU | CPU

#### Goal

The goal of this project is to implement dynamic data migration into a trace-based simulator and to evaluate its potential.

### **Prerequisites**

To successfully complete this project, you should already have the following skills and experiences.

- Very good programming skills in C++ or SystemC
- Good comprehension of a complex system
- Very good knowledge about hardware development.

#### **Contact**

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