Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Seminar

Flexible On-Chip Interconnect for Runtime Reconfigurable Inference Dataflows of Neural Networks

Modern neural networks present a challenge in computational complexity on embedded platforms. However, their structures can offer a wide range of data reuse opportunities to reduce the cost of on-chip data movement. These reuse opporunities can be exploited through different dataflows. Convolutional neural network layers can be diverse in their dimensions and their execution style (depthwise, pointwise, dilated, etc.), making some reuse opportunties more attractive than others, depending on the the properties of the layer. For an embedded hardware to make use of all the possible reuse opportunities, a flexible on-chip interconnect is necessary, which is able to change the flow of execution at runtime.

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