Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
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Seminar

Clock Recovery Circuits on FPGA Fabric

SpaceWire is a common communication standard onboard spacecraft. It uses data-strobe encoding for data transfers over a serial link. However, for a working receiver in a SpaceWire node one needs a clock recovery circuit which recovers the clock from the data-strobe encoded stream. Currently, there is only one FPGA device that has hard clock recovery macros available and that is Microsemi's RTG4. For the idea to have SpaceWire capability available on different FPGA flavors, a research on clock recovery circuits in FPGA fabric needs to be conducted. As it is a crucial part of the SpaceWire receiver where timing constraints play a vital role, therefore the clock recovery circuit design must be thought out well.

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