Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis

Generation of Hardware Traces for a Trace-Based Simulation Environment

Today's Multi-Processor System-on-Chip (MPSoCs) are getting more and more complex due to the growing amount of cores and accelerators. Hence it's not possible anymore to set runtime parameters like frequency and task distribution by design time in an optimal manner. Therefore future controllers try to make use of machine learning which is aware of the system's current state (self-awareness).

Information Processing Factory (IPF) is a global project that claims to show self-awareness across multiple abstraction levels. It represents a paradigm shift in platform design by envisioning the move towards a consistent platform-centric design in which the combination of self-organized learning and formal reactive methods guarantee the applicability of such cyber-physical systems in safety-critical and high-availability applications.

At TUM, we explore the application and implementation of machine learning algorithms in hardware to optimize the mode of operation of MPSoCs at runtime.

Therefore, we currently evaluate our research primary on FPGAs, but also by Gem5 simulations. Unfortunatelly, the FPGA evaluation causes long and quite complex developement and Gem5 simulation is time intensive when running experiments several times for different parameters or approaches.

Additionally we are developing a trace-based simulation environment. Currently the traces for it are generated in gem5.

Your task would be to generate appropriate traces directly on our FPGA-Hardware.

Towards this goal, you'll complete the following tasks:

1. Getting familiar with your Leon3-based MPSoC on a FPGA by generating a simple MPSoC and writing a first program
2. Literature research on embedded benchmarks
3. Porting different benchmarks for SparcV8
4. Enabling tracing several statistics with GRlib's 'stats'-IPcore
5. Taking traces and verifying them by comparison with gem5

Prerequisites

- Good C knowledge
- Good VHDL + Vivado knowledge
- Good MPSoC knowledge

Contact

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Advisors

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