Institute for Integrated Systems
Department of Electrical and Computer Engineering
Technical University of Munich

TI.ITI

Master Thesis

Exploring Hybrid Replacement Policies for Caches on an FPGA Prototype

Motivation

In manycore systems, caches are used to overcome the memory wall. Caches require replacement decisions owing to limited capacity. The eviction decision greatly impacts system traffic and thereby the application execution time. This emphasizes the need to explore smarter/better replacement policies.

Project Description

The goal of this project is to implement and explore the benefits of alternative replacement policies for caches on our FPGA Prototype.

Towards this goal you'll complete the following tasks:

- Investigate the source code of the Level 2 cache
- Analyze existing cache replacement policies of the Level 2 cache
- Integrate alternative hybrid replacement policies into the Level 2 cache
- Evaluate the performance of various benchmarks for different replacement schemes and architecture parameters

Prerequisites

To successfully complete this project, you should already have the following skills and experiences.

- Good understanding of MPSoCs and Cache Coherence
- Good understanding of VHDL and C
- Self-motivated and structured work style

Learning Objectives

After you have successfully completed this project, you will be able to

- Understand the challenges of cache replacement algorithms
- Perceive the practical aspects of a multi-FPGA hardware prototype

We offer you a great working experience and we encourage your creativity in solving the problem in an interesting way.

Interested? Questions? Don't hesitate to contact me! Please include a short CV, a transcript of records and a short motivation why you're interested in this work. This makes it easier to find a topic that best matches your interests.

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