

Forschungspraxis

# **Design and Implementation of a Traffic Generator Module for a Hybrid Network on Chip**

Enabled by ever decreasing structure sizes, modern System on Chips (SoC) integrate a large amount of different processing elements, making them Multi-Processor System on Chips (MPSoC). These processing elements require a communication infrastructure to exchange data with each other and with shared resources such as memory and I/O ports. The limited scalability of bus-based solutions has led to a paradigm shift towards Network on Chips (NoC) which allow for multiple data streams between different nodes to be exchanged in parallel.

In order to accurately measure the achievable data throughput and injection rates of such a NoC it is necessary to be able to generate and consume network traffic without relying on relatively slowly executed software on processing elements.

## Goal

The goal of this work is to design and implement a module that accurately generates and consumes traffic for a hybrid TDM and packet-switched NoC and reports results to a host PC, as well as to create tests to validate the behavior of the implemented hardware.

## Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- Very good programming skills in a hardware description language i.e. VHDL or (System)Verilog
- Solid Python programming skills
- At least basic knowledge of the functionality of NoCs
- Self-motivated and structured work style

## Learning Objectives

By completing this project, you will be able to:

- Understand the concept of TDM NoCs
- Design and implement a complex hardware module in SystemVerilog
- Create tests to validate hardware modules
- Document your work in form of a scientific report and a presentation

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## Advisors

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