Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Seminar

Hardware Acceleration Techniques for Virtualized Network Functions

Network traffic is known to traverse a number of different links before reaching its destination. In one way or another it is processed at each node of the network. These processing tasks range from simple IP forwarding to more complex operations like the deployment of firewalls. Network functions traditionally were realized using dedicated proprietary hardware which is now more and more replaced by commodity servers executing the same tasks in software, effectively virtualizing the network functions. Since general purpose computing equipment however is inherently slower in direct comparison, recent approaches to improve their performance attempt to support them using hardware accelerators like FPGAs, ASICs or NPUs.

The goal of this seminar topic is to investigate state of the art hardware acceleration techniques to improve virtualized network function performance.

Advisors

Franz Biersack