Master's Thesis

Evaluation of a new European FPGA technology ("Brave") for space mass memory (at Airbus in Friedrichshafen)

- Evaluation of the "Brave Large" FPGA technology in terms of the impact for current space mass memory FPGA architectures
- Perform the portability assessment of a space mass memory applications to the new FPGA technology, make use of the
available on-chip ARM Cortex R5 core if necessary
- Demonstrate the performance of the application with an implementation on the simulation tools and in hardware
- Evaluation of tool chain (Synthesis and Place and Route) for this technology
- Documentation of all the evaluation, implementation, various analysis and test results.

Advisors

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