Seminar

Survey: Power Estimation on the Electronic System Level

To cope with the increasing complexity of modern electronic systems, today's system designers rely heavily on the use of high-abstraction models of the targeted hardware system. A typical example of such a model are so-called Virtual Prototypes (VP). The abstraction level itself is loosely defined as the Electronic System Level (ESL).

ESL offers high simulation speed, and as such enables the exploration of different system architectures already during early stages of the design phase. However, detailed information about the system's power performance is usually not provided. Especially for the design of embedded systems this depicts a major drawback, as power requirements play an important role during the consideration of different system architectures. To solve this problem, several approaches to estimate power consumption on ESL have been proposed in the literature.

Example paper:

- Abdel Haleem et al.; "TLM Virtual Platform for Fast and Accurate Power Estimation", 2017
- Rethinagiri et al.; "PETS: Power and Energy Estimation Tool at System-Level", 2014

Contact

conrad.foik@tum.de

Advisors

Conrad Foik