Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis

Statistical-based Switching Activity Estimation in the PyMTL3 Framework

In System on Chip (SoC) design, power consumption gets increasingly important (e.g. due to increasing complexity of the devices and contrary, due to the growing number of mobile applications). Although precise gate-level simulation methods exist, they are not feasible for larger designs. Therefore, less accurate, but faster methods have been developed. For dynamic power dissipation, the switching activity of a design is crucial (beside technological parameters). For example, probabilistic switching activity estimators propagate static and dynamic switching activities of primary inputs through the design on a high level to obtain its switching activity [1]. Other methods use Monte-Carlo principles to obtain average power estimates by simulating a large number of random inputs (called statistical-based methods). Furthermore, the use of machine learning has been proposed for high-level power estimation in recent work. [2]

Various platforms exist for the developement of the SoC itself. On one side, classic, commercial tools exist for the design and synthesis flow. Hardware description languages (HDL), like VHDL or Verilog, exist for an efficient modeling and design process. In recent research, also open source solutions in EDA are developed. For example, the PyMTL(3) framework should provide hardware modeling capabilities on various levels of system design [3]. This Python(3)-based framework consists of an own HDL, an API to the elaborated design and the possibility to develop custom extension programs (passes called) for further investigation. This includes for example already various passes for simulations.

The objective of the thesis should be to develop a statistical-based switching activity pass in the PyMTL3 framework. This includes the literature research for statistical-based switching activity/ power modeling methods, the familiarization with the PyMTL3 framework and the development of a suitable method in a PyMTL3 pass.

[1] Schneider, P. H., Schlichtmann, U., & Wurth, B. (1996). Fast power estimation of large circuits. IEEE Design & Test of Computers, 13(1), 70-78.

[2] Nasser, Y., Lorandel, J., Prévotet, J. C., & Hélard, M. (2020). RTL to Transistor Level Power Modelling and Estimation Techniques for FPGA and ASIC: A Survey. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

[3] Jiang, S., Pan, P., Ou, Y., & Batten, C. (2020). PyMTL3: a Python framework for open-source hardware modeling, generation, simulation, and verification. IEEE Micro, 40(4), 58-66.

Prerequisites

- Experience in Python
- Knowledge in Hardware Description Languages (HDL)
- Interest in Power Modeling of Digitial Circuits/ SoCs

Contact

If you are interested in the topic, please feel free to contact me at: philipp.fengler@tum.de

Advisors

Philipp Fengler