Seminar

A HW/SW Co-Verification Framework for SystemC

To cope with the increasing complexity of modern embedded systems today's design processes often rely on electroinic system level (ESL) modeling. These high abstraction models are frequently refered to as virtual prototypes (VP) and typically implemented with a C++ extension, called SystemC.

With the help of VP-based simulations, the hardware (HW) and software (SW) components of a given system, can be designed and verified early on and alongside each other. This parallelized, interactive processes are refered to as HW/SW co-design and co-verification, respectively.

However, existing verification techniques on ESL/SystemC-level are still mostly ad-hoc and non-systematic. This limits the maintainability and reusability, as well as the automation capacity of the HW/SW co-verification approaches.

During this project, a proposal for a more systematic SystemC verification framework shall be investigated.

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