Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Master's Thesis

RISCV Multi-level Simulation Setup for Fast RTL Accurate Evaluation

RTL Accurate simulation based test beds are needed to design reliable fault tolerance mechanisms to boost soft error resilience of embedded systems. However, pure RTL simulations of embedded SW (e.g. via ModelSim) is prohibitively slow. To speed up RTL simulations, this work would look into the possibility of switching methodologies between a higher level ISS model and an equivalent RTL model. Initial focus would be on RISCV targets.

Prerequisites

Concepts in Digital Design, Computer Architecture

Good knowledge of C++, HDL

Contact

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Advisors

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