Enabled by ever decreasing structure sizes, modern System on Chips (SoC) integrate a large amount of different processing elements, making them Multi-Processor System on Chips (MPSoC). These processing elements require a communication infrastructure to exchange data with each other and with shared resources such as memory and I/O ports. The limited scalability of bus-based solutions has led to a paradigm shift towards Network on Chips (NoC) which allow for multiple data streams between different nodes to be exchanged in parallel.

In order to implement a safety-critical real-time application on such an MPSoC, the NoC must fulfill certain requirements: it must ensure that no critical data gets lost, all critical data gets delivered within a certain deadline, and other applications cannot interfere with the critical application. And all this must be guaranteed even in case of a fault in the NoC. Furthermore, to offload the processing elements and to decrease the amount of required buffers, DMA transfers should be supported.

**Goal**

The goal of this thesis is to implement a DMA Controller in a Network Interface supporting a hybrid Time-Division Multiplexed (TDM) and packet-switched NoC that provides protection switching for critical traffic and to create tests to validate the behavior of the implemented hardware.

**Prerequisites**

To successfully complete this project, you should already have the following skills and experiences:

- Very good programming skills in a hardware description language i.e. (System)Verilog or VHDL
- Solid Python programming skills
- At least basic knowledge of the functionality of NoCs
- Self-motivated and structured work style

**Learning Objectives**

By completing this project, you will be able to

- understand the concept of TDM NoCs and DMA transfers
- design and implement a complex hardware module in SystemVerilog
- create tests to validate hardware modules
- document your work in form of a scientific report and a presentation

**Advisors**

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