Implementation of a Sensitized Path PUF on Xilinx FPGA

Physical Unclonable Functions (PUFs) exploit manufacturing process and physical environmental variations to generate unique signatures. These signatures can be used for key generation or in challenge-response protocols.

In this work, a Sensitized Path PUF should be implemented and evaluated on XILINX FPGA. This PUF type uses the configuration capabilities of LUTs on FPGAs to increase the amount of extracted entropy per area compared to, e.g. standard RO implementations.

During the course of the thesis, the following should be covered:

- Get familiar with sensitized path PUFs
- Plan and conduct the implementation on a Basys3 Board
- Test the implementation with state of the art quality metrics for PUFs.

This work can be conducted in German or English. Please contact the thesis supervisor for further details. In case of a high quality of the work, results might be published.

References:

- L. Feiten, M. Sauer, B. Becker; "Implementation of Delay-Based PUFs on Altera FPGAs"; HOST 2017; https://doi.org/10.1007/978-3-319-44318-8_11

Prerequisites

- Good VHDL skills

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