Master's Thesis

SW Implementation for NR FEC

- Study of the NR FEC Specifications (i.e. Polar Codes and LDPC Codes)
- Study of the Decoding Algorithms for the NR FEC Codes
- Implementation of the NR FEC Codes on General Purpose Processors using SIMD technology
- Profiling of the implementation with respect to latency, throughput and memory footprint

Prerequisites

- University degree in computer engineering or comparable course of study
- Profound knowledge on state of the art processor architectures
- Profound knowledge on state of the art programming (making use of SIMD and multi-core technologies)
- Profound knowledge on state of the art operating systems (such as Windows or Linux)
- Good communication skills
- Self-motivated and self driving personality
- Ability to work in an inter-cultural working Environment

Advisors

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