Master Thesis

Evaluating Shared Memory Workloads on a DSM-based MPSoC using Region Based Cache Coherence

Motivation
Providing hardware coherence for modern tile-based MPSoCs requires additional area. As a result, this does not scale with increasing tile counts. As part of the Invasive Computing project, we introduced Region Based Cache Coherence (RBCC) which is a scalable approach that provides on-demand coherence. RBCC enables users to dynamically create/destroy coherency regions based on application requirements. The next step is to execute and evaluate real world shared memory workloads on a DSM system using RBCC support.

Project Description
The goal of this project is to explore, adapt and evaluate shared memory workloads using RBCC on our FPGA prototype.

Towards this goal you’ll complete the following tasks:
- Investigate existing shared memory programming primitives
- Adapt shared memory workloads to be executable on a DSM System
- Evaluate RBCC using the SPLASH-2 benchmarks on an FPGA platform

Prerequisites
To successfully complete this project, you should already have the following skills and experiences.
- Very Good VHDL Skills
- Good C/C++ Skills
- Good understanding of MPSoCs and Cache Coherence Schemes
- Self-motivated and structured work style

Learning Objectives
After you have successfully completed this project, you will be able to
- Understand the challenges of cache coherence in multi-core systems
- Understand the work flow from software-to-hardware

We offer you a great working experience and we encourage your creativity in solving the problem in an interesting way.

Interested? Questions? Don't hesitate to contact me! Please include a short CV, a transcript of records and a short motivation why you're interested in this work. This makes it easier to find a topic that best matches your interests.

Akshay Srivatsa
Chair of Integrated Systems
Arcisstraße 21, 80333 Munich
Tel. +49 89 289 22963
srivatsa.akshay@tum.de
www.lis.ei.tum.de