Chair of Security in Information Technology
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Assistant (Student)

# Working Student: Chip Design for Security Applications (AISEC)

Fraunhofer AISEC and TU Munich are collaborating in designing security chip prototypes for various research projects. You have the opportunity to work with a team of researchers on realizing innovative security solutions on hardware circuits. During your work, you will both learn valuable skills related to the different stages of chip design and have the opportunity to contribute to cutting edge research, e.g. Physical Unclonable Functions, Post Quantum Cryptography, Hardening of cryptographic algorithms, … . This job is an ideal starting point for a future career in chip design and information security.

## Prerequisites

* One of the following and the motivation to learn the other:
  Experience with at least one hardware description language, e.g. (System) Verilog or VHDL
  Experience with embedded software development, e.g. C, Assembly (ARM/RISC-V), Rust
* Experience with Python
* Experience with Linux
* Motivation for learning more about chip design
* Motivation for contributing to research in hardware security

## Contact

Please send an email with:
* A short CV
* A short cover letter
* Your last grading sheet
* 3-5 dates, which fit to your schedule, for a meeting.

Felix Oberhansl, felix.oberhansl@aisec.fraunhofer.de

## Advisors

Georg Sigl
Felix Oberhansl (Fraunhofer AISEC)