

Forschungspraxis, Assistant (Student), Master's Thesis, Bachelor's Thesis

Exploring netlist representations for netlist RE

Reverse engineering of silicon hardware designs is an interesting task for various applications in science and industry, such as patent infringement detection, security analysis or hardware trojan detection.

One of the most challenging tasks is to go from the flat netlist, that is a graph of logic gates and wires between them, to a high level description of the design.

In this work, you will analyze and compare different methods for representing a netlist and the benefits and problems when analyzing the netlist using the different representations

Prerequisites

The following list of prerequisites is neither complete nor binding, but shall give you an idea, what the topic is about.

- Sufficient knowledge in a python to use our existing framework
- Basic knowledge of a hardware description language such as vhdl or verilog to understand what you are analyzing
- Basic knowledge in graph theory, algorithms etc. to cope with problems on the way.

Contact

If you are interested in this topic, don't hesitate to ask for an appointment via

alex.hepp@tum.de

Please include a grade report and a CV, so I can evaluate different focus areas to fit your experience.

Advisors

Alexander Hepp