

Ingenieurspraxis, Forschungspraxis

# Automation of Sequential Locking Scheme Insertion

The aim of sequential gate-level netlist reverse engineering is to identify and extract the control logic out of a gate-level design netlist. Thereto, first, the registers have to be classified into state and data registers, i.e. registers which belong to the control logic and registers which do not belong to the control logic. The identified state registers are then used as a starting point to extract the finite state machine (FSM) [1]. The extraction of the control logic might support an attacker to retrieve secret design information or enable product piracy. Therefore, a number of sequential locking techniques, like for example Harpoon [2], are already developed which aim to obfuscate FSMs and prevent control logic extraction. Usually, a secret locking key has to be applied such that the correct FSM behavior is achieved.

In this work, first an already existing tool of the Neta toolset [3] for inserting a sequential locking scheme should be applied and analyzed. Possible helper tools to make the usage of the existing tool easier and more generally applicable should be developed. Finally, a concept for an automatic insertion of different sequential locking methods should be determined and implemented.

## References:

- [1] McElvain, K. S. Methods and apparatuses for automatic extraction of finite state machines Google Patents, 2001
- [2] Chakraborty, R. S. & Bhunia, S. HARPOON: an obfuscation-based SoC design methodology for hardware protection IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE, 2009, 28, 1493-1502
- [3] Meade, T.; Portillo, J.; Zhang, S. & Jin, Y. NETA: when IP fails, secrets leak Proceedings of the 24th Asia and South Pacific Design Automation Conference, 2019, 90-95

## Prerequisites

- Basic knowledge in the synthesis flow
- Interested in graph theory and automata theory

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