

Bachelor's Thesis

# Modeling of errors in Netlists

In a realistic Reverse Engineering Scenario, where a chip is delayered, imaged and then analysed, errors during earlier steps will hinder the later analysis. In order to better understand the effect of these errors on the steps for reverse engineering, this work should model errors which can occur during reverse engineering, and analyse their effect.

## Prerequisites

Idealy:

1. Python / C
2. VHDL / Verilog

## Contact

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