Fault Tolerance in Local Rank Modulation

Non-volatile memories (NVMs) are electronic data-storage technologies that do not require a continuous power supply to retain data; unlike traditional magnetic or optical media, they do not utilize mechanically movable components and can therefore offer better performance, and allow for three-dimensional scaling of storage devices. Under most realistic workloads, they also offer better energy efficiency.

However, these technologies also feature imbalances in behavior, performance and consequences, between the processes of reading data and writing it. To wit, in memory cells which represent data by the level of held charge (traditionally allowing for representation of several logical levels), the process of charge-injection is a simple and efficient, whereas charge-depletion is both technically complex (requiring the depletion of entire blocks of cells) and destructive, a main driver of cell-degradation over the device’s life cycle.

Different coding theoretic approaches have been explored to alleviate this imbalance, including coding schemes that delay charge-depletion cycles [1], [2]. This project will build on the work done in [2], by calculating the asymptotic behavior of the number of realizable permutation sequences, when those are restricted to belong to a single Kendall-tau error-detecting code. Possible extensions will be general error-correction capabilities, as well as general window-lengths.


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