

Master's Thesis

Simulation of Improved Staircase Code Decoding

Staircase codes, as introduced in 2011 by Smith et. al. [1], are a hardware friendly code design for error correction in optical communication systems. However, the choices of parameters such as block size and code rate that achieve a desired output bit error rate are limited by the error floor of the decoder. A new and improved decoder has been devised [2], allowing for staircase codes with a scope of new parameters to be considered for optical communication. While estimations show the significant improvements, the high throughput required to simulate the error floor can only be achieved with an efficient and parallelisable implementation. The main goal of the thesis is the implementation in VHDL and simulation on an FPGA of the new decoder in order to provide further evidence for the estimated performance.

[1] <https://arxiv.org/abs/1201.4106>

[2] <https://arxiv.org/abs/1704.01893>

Prerequisites

interest in channel coding, knowledge in VHDL

Advisors

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