

Bachelor's Thesis, Forschungspraxis

# Implementation of Fault-Injection & Fault-Detection Mechanisms in a Time-Division Multiplexed Network on Chip

Enabled by ever decreasing structure sizes, modern System on Chips (SoC) integrate a large amount of different processing elements, making them Multi-Processor System on Chips (MPSoC). These processing elements require a communication infrastructure to exchange data with each other and with shared resources such as memory and I/O ports. The limited scalability of bus-based solutions has led to a paradigm shift towards Network on Chips (NoC) which allow for multiple data streams between different nodes to be exchanged in parallel.

To implement safety-critical real-time applications on such an MPSoC, the NoC must be fault-tolerant. In order to fulfill this requirement, it is necessary to first detect a fault in the system. Furthermore, to test this requirement, it is necessary to be able to inject errors into the system at random times and places.

## Goal

The goal of this thesis is to implement a fault-injection and a fault-detection mechanism in a Time-Division Multiplexed (TDM) NoC and to create tests to validate the behavior of the hardware models.

## Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- At least basic programming skills in a hardware description language i.e. VHDL or (System)Verilog
- Solid Python programming skills
- At least basic knowledge of the functionality of NoCs
- Self-motivated and structured work style

## Learning Objectives

By completing this project, you will be able to

- understand the concept of TDM NoCs
- understand the concept of fault-detection in hardware
- create and extend hardware modules in SystemVerilog
- create tests to validate hardware modules

- document your work in form of a scientific report and a presentation

## Contact

Max Koenen  
Room N2118  
Tel. 089 289 23084  
max.koenen@tum.de

## Advisors

Max Koenen