Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Master's Thesis

Design and Implementation of a Fault-Tolerant Low-Throughput Broadcast Control & Management Network for System on Chip

Enabled by ever decreasing structure sizes, modern System on Chips (SoC) integrate a large amount of different processing elements, making them Multi-Processor System on Chips (MPSoC). These processing elements require a communication infrastructure to exchange data with each other and with shared resources such as memory and I/O ports. The limited scalability of bus-based solutions has led to a paradigm shift towards Network on Chips (NoC) which allow for multiple data streams between different nodes to be exchanged in parallel.
One way of organizing the access to such a NoC is by using Time-Division Multiplexing (TDM) which allows to give service guarantees. However, such a TDM NoC must be configured before it can be used which requires a reliable configuration network.

Goal

The goal of this thesis is to implement a reliable broadcast configuration network that can be used to configure the routers and network interfaces of a TDM NoC and to create tests to validate the implemented hardware.

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- Good programming skills in a hardware description language i.e. VHDL or (System)Verilog
- Good knowledge of on-chip communication
- Solid Python programming skills
- At least basic knowledge of the functionality of NoCs
- Self-motivated and structured work style

Learning Objectives

By completing this project, you will be able to

- understand the concept of TDM NoCs
- create and extend hardware modules in SystemVerilog
- create tests to validate hardware modules
- document your work in form of a scientific report and a presentation

Contact

Max Koenen
Room N2118
Tel. 089 289 23084
max.koenen@tum.de

Advisors

Max Koenen