Forschungspraxis

**IPF1 Demonstrator to visualize classifier generation using Genetic Algorithms for LCTs**
Reinforcement learning (RL) has been widely used for run-time management on multi-core processors. RL-based controllers can adapt to varying emerging workloads, system goals, constraints and environment changes by learning from their experiences.

Learning classifier tables (LCTs) are hardware based machine learning entities that are applied in our IPF project as low level controllers for DVFS. LCTs inherit the concept from learning classifier systems which is a rule based machine learning system.

In this work, you will

1. Develop a demonstrator to visualize classifier generation in LCTs.
2. Write low level embedded software in C to communicate between the Matlab GUI and software running on the FPGA.
3. Understand Implementation of LCTs on the Leon3 platform running on Virtex7 FPGA.

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:
- Good VHDL, Matlab and C programming skills
- Good understanding of MPSoCs
- Self-motivated and structured work style
- Knowledge of machine learning algorithms (LCS)

Contact

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