Fine granular Page Preloading Mechanism on an FPGA Prototype

Their main advantages are an easy design with only 1 Transistor per Bit and a high memory density make DRAM omnipresent in most computer architectures. However, DRAM accesses are rather slow and require a dedicated DRAM controller that coordinates the read and write accesses to the DRAM as well as the refresh cycles. In order to reduce the DRAM access latency, memory prefetching is a common technique to access data prior to their actual usage. However, this requires sophisticated prediction algorithms in order to prefetch the right data at the right time.

The Goal of this thesis is to refine an existing DRAM preloading mechanism on an FPGA based prototype platform. Instead of preloading a whole memory page in a single atomic operation, the refinement should lead to a fine-granular page preloading, i.e. loading multiple small fractions of a page step by step while allowing regular memory accesses to be prioritized intermediately.

Towards this goal, you'll complete the following tasks:
1. Understanding the existing Memory Access and Preloading mechanism
2. VHDL implementation of the refined preloading functionalities
3. Write and execute small baremetal test programs
4. Analyse and discuss the performance results

Prerequisites

- Good Knowledge about MPSoCs
- Good VHDL skills
- Good C programming skills
- High motivation
- Self-responsible workstyle

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