Bachelor's Thesis

Developement and Evaluation of a Hardware Thread Scheduler on a FPGA

In modern computing systems, efficient resource management is crucial for maximizing performance and ensuring fair resource allocation among tasks. One critical aspect of resource management is thread scheduling, which involves determining the order and timing of execution for concurrent tasks or threads. In this project, we propose to implement a hardware-based thread scheduler on a Field-Programmable Gate Array (FPGA).

Objectives:

- Design and implement a hardware-based thread scheduler
- Integrate the scheduler into existing FPGA prototype
- Test and Evaluate the design

Tasks include:

1. Understanding the underlying software mechanisms for thread scheduling
2. Designing the hardware scheduler
3. Implementing the design in HDL
4. Testing the design

Implementing a hardware thread scheduler on an FPGA offers significant advantages in terms of performance, efficiency, and inter-process communication. This project aims to explore the design, implementation, and evaluation of such a scheduler.

Advisors

Tim Twardzik