Hardware Interrupt Generation for Smart Servers

With the advent of research on the next generation of mobile communications 6G, we are engaged in exploring architecture extensions for Smart Network Interface Cards (SmartNICs). To enable adaptive, energy-efficient and low-latency network interfaces, we are prototyping a custom packet processing pipeline on FPGA-based NICs, partially based on the open-nic project (https://github.com/Xilinx/open-nic).

To improve the performance and energy efficiency of a modern server, SmartNICs can be used to preprocess incoming packets and gather characteristics on traffic and processing requirements. This information can be used to change the processing behavior of the server and react to the dynamic network and processing requirements. To do so, the server has to be notified of detected events using an interrupt.

The goal of this work is to implement hardware-based interrupt generation in an FPGA-based SmartNIC using HDL and PCIe IP cores, registering the interrupt with the Linux interrupt driver as well as writing a suitable ISR (interrupt service routine). This mechanism should be functionally verified in a hardware testbed and evaluated regarding the latency of the interrupt. Additionally, the work could be extended to include setting the core affinity of an interrupt and generating interrupts destined for specific CPU cores.

Prerequisites

- Programming skills in VHDL/Verilog and C (and Python)
- Practical experience with FPGA Design and Implementation
- Good Knowledge of computer architecture and low-level software / drivers
- Comfortable with the Linux command line and bash

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