Implementation and Evaluation of Hardware Match-Action Tables on FPGA

With the advent of research on the next generation of mobile communications 6G, we are engaged in exploring architecture extensions for Smart Network Interface Cards (SmartNICs). To enable adaptive, energy-efficient and low-latency network interfaces, we are prototyping a custom packet processing pipeline on FPGA-based NICs, partially based on the open-nic project (https://github.com/Xilinx/open-nic).

Incoming packet flows should be differentiated and differently processed, which is typically solved with match-action tables (MATs). MATs match on a certain packet condition (e.g. packet header 5-tuple) and execute an according action (e.g. dropping, forwarding or modifying the packet). A recent Xilinx IP core implements MATs that can be programmed with P4, a programmable packet processing language gaining momentum in networking. The goal of this work is to investigate the implementation of MATs in hardware, integrate them into our current HDL design based on open-nic and test and evaluate the results.

Prerequisites

- Programming skills in VHDL/Verilog and C (and Python)
- Practical experience with FPGA Design and Implementation
- Good Knowledge of computer networks, OSI layer model and protocols
- Preferably basic knowledge of P4 packet processing language

Contact

Marco Liess, M. Sc.

Tel.: +49.89.289.23873
Raum: N2139
Email: marco.liess@tum.de

Advisors

Marco Liess