Hardware Queue-to-Core Pinning for Load Balancing using SmartNICs

With the advent of research on the next generation of mobile communications 6G, we are engaged in exploring architecture extensions for Smart Network Interface Cards (SmartNICs). To enable adaptive, energy-efficient and low-latency network interfaces, we are prototyping a custom packet processing pipeline on FPGA-based NICs, partially based on the open-nic project (https://github.com/Xilinx/open-nic).

Load balancing is a challenging task in modern data centers and servers, as the number of processing cores rises (96 cores in recent AMD Epyc platforms) and the packet processing workload should be distributed equally among them. To assist this process, incoming packet flows should be differentiated and assigned to different queues already in the NIC hardware. These queues must then be pinned to different processor cores to ensure the hardware load-balancing algorithm works correctly.

The goal of this work is to implement the queue assignment in the FPGA SmartNIC platform using HDL, configuring the NIC driver to use the correct queues, and pinning the processing of the queues onto different CPU cores. Further, functional verification as well as performance evaluation should be done on the system.

Prerequisites

- Programming skills in VHDL/Verilog and C (and Python)
- Practical experience with FPGA Design and Implementation
- Good Knowledge of computer networks, OSI layer model and protocols
- Comfortable with the Linux command line and bash

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