Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Master's Thesis

Extensions & Performance Benchmarks of a CAPI-based Network Interface Card

With ever-increasing network data rates, the data transfer between network interface card (NIC) and the host system has a decisive impact on the achievable application performance. To fully exploit the host system's CPU capacity for application processing, it is important to minimize I/O processing overheads. In this project, we want to extend the implementation and optimize the performance of an FPGA-based NIC that is connected to the host system with the Coherent Accelerator Processor Interface (CAPI) [1] for IBM POWER8 Systems.

In a previous project an initial implementation of the CAPI-based NIC was developed using the CAPI Storage, Network and Analytics Programming (SNAP) framework [2]. The goal of this project is to integrate the physical network interfaces in the design, as well as to identify and mitigate performance bottlenecks.

[1] https://developer.ibm.com/linuxonpower/capi/

[2] https://openpowerfoundation.org/blogs/capi-snap-simple-developers

Towards this goal you will complete the following tasks:

- Analyze source code and working principles of the existing NIC implementation
- Getting familiar with CAPI and the CAPI SNAP framework
- Integrate an Ethernet Media Access Controller (MAC) IP core into the FPGA design
- Benchmark throughput and latency of FPGA-to-host communication through simulations and measurements
- Identify performance bottlenecks, propose and implement improvements
- Extend the design to make use of multiple RX/TX queues for multi-core processing

Prerequisites

To successfully complete this project, you should already have several of the following skills and experiences:

- Knowledge of a hardware description language such as Verilog and/or VHDL
- Hands-on FPGA development experience
- Solid C programming skills
- Proficiency using Linux

- Self-motivated and structured work style

Learning Objectives

By completing this project, you will be able to

- understand the basic working principles of NICs, as well as FPGA-host communication mechanisms
- apply your theoretical knowledge to an implementation consisting of both hard- and software parts
- document work in a scientific report form and in a presentation

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