Bachelor's Thesis

Development of a Priority-Aware Scheduler for Packet-Processing Architectures

FlexPipe is a packet-processing architecture where offloads are arranged sequentially in the order that they are intended to be used. Each offload contains flexible forwarding logic that bypasses its processing units if their functionality is not needed by an incoming packet in order to reduce latency. Furthermore, it contains a scheduler that steers traffic to the least loaded processing unit.

The goal of this project is to extend FlexPipe with priority awareness in order to ensure that high-priority packets are privileged when contention for shared resources occurs. The first step is to design a scheduler that doesn’t consider only the current load of the available processing units, but also the priority of incoming packets by forwarding packets with specific priorities to specific processing units. The second step is to design a traffic arbiter that first forwards high-priority packets when multiple processing units have finished processing a packet. It also decides whether packets that bypass the offload or those that use it are forwarded to the next offload based on their priorities. The design should be implemented in Verilog and integrated into the existing packet-processing architecture. Moreover, it should be evaluated via behavioral simulations in Vivado.

Advisors

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