Master's Thesis

SmartNIC Enhancements for Network Node Resilience

The Chair of Integrated Systems participates in the DFG Priority Program “Resilient Connected Worlds” by the German Research Foundation (SPP 2378). Our goal is to investigate which resilience functions, that conventionally are provisioned by the central compute resources of Internet Networking or Compute Nodes, can meaningfully be migrated onto the Network Interface Card (NIC). By inspecting packet streams at full line rate (10 – 40 Gbps) a set of resilience functions, such as access shields against a known set of traffic flows or redundant flow processing for a selected and configured number of flows, shall be offloaded from centralized compute resources and offered in a more performant and energy-efficient manner. Flows are identified by their so-called 5-tuple consisting of source-/destination IP addresses and transport protocol ports as well as the protocol field of the IP packet header.

During the Bachelor/Master Thesis, you will develop VHDL code for realizing one or more of the SmartNIC Resilience building blocks: 5 tuple address matching against a preconfigured set of addresses, perform the packet duplication for delivery to different processor cores or threads, investigate methods to flexibly perform the address match on the entire or a variable subsection of the 5 tuple array.

Prerequisites

- VHDL coding, synthesis and FPGA prototyping
- Broadband communication or Internet Networking Technologies, in particular OSI Layer packet header formats
- Digital circuit design

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