Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
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Bachelor's Thesis

Optimization of Hardware Assisted Futex Implementation on Zynq Ultrascale+ MPSoC

An upcoming trend in the development of compute architecture can be seen over the last few years. Next to the ever-increasing number of cores in one system, dedicated hardware accelerators for a specific task are getting increasingly widespread. These hardware accelerators are designed to outperform a general-purpose CPU resulting in a performance increase as well as a relief of the CPU. One challenging task for utilizing the accelerator efficiently is the implementation of a performant interface in addition to a way to notify the issuing task after completing the task in a hardware accelerator. The proof of concept for hardware accelerating this notification is accomplished by integrating the framework, software- as well as hardware-wise, into a heterogeneous architecture simulated in a full system simulation using Gem5. This work focuses on optimizing a hardware prototyping environment to further evaluate the hardware accelerator concepts not only via a simulation but also through a real hardware platform. The used hardware platform is a Xilinx Zynq board. This features a heterogeneous ARM multicore setup directly integrated into the ASIC, combined with programmable logic in the FPGA part of the chip. On the software side, a similar setup as in the simulation environment is used including the use of Linux as the operating system.

Advisors

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