

Forschungspraxis

Development and Evaluation of a Crossbar for Packet Processing Architectures

The goal of this project is to design, implement and evaluate a crossbar. The crossbar should be compatible with AXI4-Stream and support at least two arbitration modes when multiple initiators want to access the same target: round-robin and priority-based. It should introduce no idle clock cycles when switching from a waiting state to a forwarding state and when switching between different initiators that want to access the same target.

The crossbar should be implemented in Verilog and integrated into an existing packet processing architecture. Furthermore, it should be compared to other interconnects in terms of throughput and latency via behavioral simulations in Vivado. Optionally the design can be implemented and tested on FPGA.

Advisors

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