Forschungspraxis

Investigation and Implementation of Approximate Dividers for FPGA

Approximate computing is an emerging design paradigm that trades in accuracy for resource consumption, i.e. a certain inaccuracy of the calculations is allowed with the goal of reducing the overall resource consumption of the implemented design. One branch in this research field focuses on the approximation of arithmetic units, such as adders, subtractors, multipliers, and dividers. In this research internship, approximate dividers suitable for implementation on FPGA should be investigated.

The research internship starts with a literature research about state-of-the-art approximate dividers. Relevant literature must be searched and surveyed. Afterwards, the most promising approximate divider designs have to be selected based on the literature research. These designs must then be implemented in VHDL targeted for an FPGA design. Finally, a rudimentary evaluation of the implemented dividers has to be performed.

Prerequisites

The student should have the following skills in order to successfully complete the research internship:

- Good ability to understand technical and scientific literature (e.g IEEE or ACM papers)
- Analytical thinking
- Good programming skills in VHDL
- The ability to work independently
- High motivation
- Previous experience with approximate computing is helpful, but not essentially required.

The student can work on the research internship remotely from his home office.

Contact

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Advisors

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