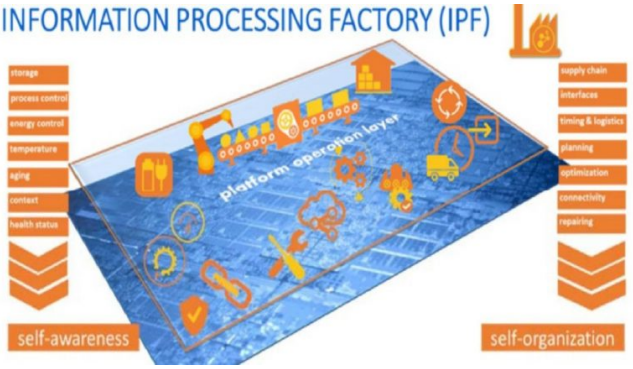
Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Forschungspraxis

Development of a Learning Engine Debugger



Today's Multi-Processor System-on-Chip (MPSoCs) are getting more and more complex due to the growing amount of cores and accelerators. Hence it's not possible anymore to set runtime parameters like frequency and task distribution by design time in an optimal manner. Therefore future controllers try to make use of machine learning which is aware of the system's current state (self-awareness).

Information Processing Factoriy (IPF) is a global project that claims to show self-awareness across multiple abstraction levels. It represents a paradigm shift in platform design by envisioning the move towards a consistent platform-centric design in which the combination of self-organized learning and formal reactive methods guarantee the applicability of such cyber-physical systems in safety-critical and high-availability applications.

At TUM, we explore the application and implementation of machine learning algorithms in hardware to optimize the mode of operation of MPSoCs at runtime.

Towards this goal, you'll complete the following tasks:

1. Understand state of the art debugg mechanisms, which overcome the off-chip bottle neck
2. Investigate error symptoms, their causes and possible metics to prove them for LCTs.
3. Design and implement the debugger (VHDL on HW side + maybe Matlab on Host side)
4. Verify your design

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- Excellent knowledge about LCTs
- Good VHDL Skills
- Good C / C ++ Skills
- Good Matlab Skills
- Good Understanding of MPSoCs
- Self-motivated and structured work style

Contact

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