Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Master's Thesis

Design of a RISC-V MPSoC with Autonomic Layer (IPF)

Today's Multi-Processor System-on-Chip (MPSoCs) are getting more and more complex due to the growing amount of cores and accelerators. Hence it's not possible anymore to set runtime parameters like frequency and task distribution by design time in an optimal manner. Therefore future controllers try to make use of machine learning which is aware of the system's current state (self-awareness).

Information Processing Factoriy (IPF) is a global project that claims to show self-awareness across multiple abstraction levels. It represents a paradigm shift in platform design by envisioning the move towards a consistent platform-centric design in which the combination of self-organized learning and formal reactive methods guarantee the applicability of such cyber-physical systems in safety-critical and high-availability applications.

At TUM, we explore the application and implementation of machine learning algorithms in hardware to optimize the mode of operation of MPSoCs at runtime.

Currently we use a Leon3 setup, but more and more of recent research on SoC design including CPUs is done using the open RISC V instruction set. Due to this fact the community and the amount of available tools is constantly increasing, which is a significant advantage over other platforms like SparcV8.

For this reason we want to port our current Leon3 design to this new platform.

Towards this goal the following tasks need to be done in this master thesis:

1. There exist several open source implementations of RISC V Cores which need to be compared in a first step.
2. Afterwards, a first MPSoC needs to be synthesized using the most promising implementation. A first goal on this MPSoC is to run a simple ‘Hello World’ using all cores.
3. The final step afterwards would be to attach our autonomic machine learning layer to this MPSoC in order to get a self-aware system doing DVFS and task migration autonomously.

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- Good VHDL and Verilog Skills
- Basic Knowledge of RISC V specialities
- Good Understanding of MPSoCs
- Self-motivated and structured work style
- opional: Basic Knowledge of Machine Learning

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