Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Forschungspraxis, Assistant (Student), Master's Thesis, Bachelor's Thesis

Development of an I/O Tile for an MPSoC Demonstrator Fea- turing a Hybrid TDM and Packet-Switched NoC

Enabled by ever decreasing structure sizes, modern System on Chips (SoC) integrate a large amount of different processing elements, making them Multi-Processor System on Chips (MPSoC). These processing elements require a communication infrastructure to exchange data with each other and with shared resources such as memory and I/O ports. The limited scalability of bus-based solutions has led to a paradigm shift towards Network on Chips (NoC) which allow for multiple data streams between different nodes to be exchanged in parallel.
Each SoC also needs a way to communicate with its environment, typically provided in form of an I/O tile. For an MPSoC demonstrator on an FPGA it is necessary to implement such an I/O tile to enable data exchange between the applications running on the FPGA and a host PC.

Goal

The goal of this work is to implement an I/O tile for an MPSoC demonstrator on an FPGA and enable data exchange between the applications running on the FPGA and a host PC.

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:

- Good programming skills in a hardware description language i.e. (System)Verilog or VHDL
- Good programming skills in C
- Solid Python programming skills
- At least basic knowledge of the functionality of NoCs
- Self-motivated and structured work style

Learning Objectives

By completing this project, you will be able to

- Understand the concept of TDM NoCs
- Create and extend hardware modules in SystemVerilog
- Create tests to validate hardware modules
- Document your work in form of a scientific report and a presentation

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