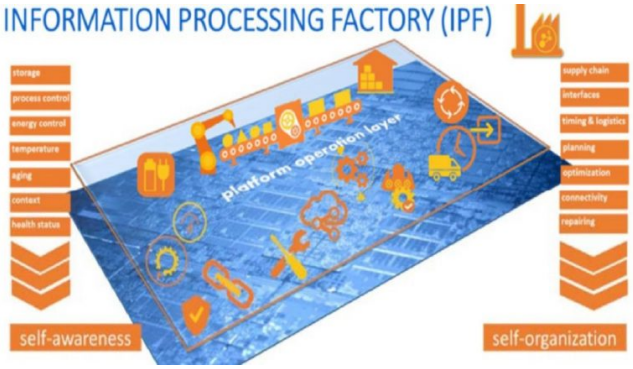
Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis, Forschungspraxis, Assistant (Student)

HW-SW interface design for a self-aware SoC paradigm based on hardware machine learning (IPF)



As today's Multi-Processor System-on-Chip (MPSoCs) are getting more and more complex due to the growing amount of cores and accelerators. Hence it's not possible anymore to set runtime parameters like frequency and task distribution by design time in an optimal manner. Therefore future controllers try to make use of machine learning which is aware of the system's current state (self-awareness).

Information Processing Factoriy (IPF) is a global project that claims to show self-awareness across multiple abstraction levels. It represents a paradigm shift in platform design by envisioning the move towards a consistent platform-centric design in which the combination of self-organized learning and formal reactive methods guarantee the applicability of such cyber-physical systems in safety-critical and high-availability applications.

At TUM, we explore the application and implementation of machine learning algorithms in hardware to optimize the mode of operation of MPSoCs at runtime.

Towards this goal, you'll complete the following tasks:
1. Understand the current implementation of Learning Classifier Tables (LCT) and Supervisory Control as well as their communication with SW in VHDL.
2. Design and implement a new HW-SW interface which supports new features and functionalities on the FPGA.
3. Develop a software API to utilize the functionalities implemented in hardware.
4. Test your new HW-SW interface.

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:
- Good VHDL Skills
- Good C / C ++ Skills
- Good Understanding of MPSoCs
- Self-motivated and structured work style
- opional: basic knowledge of machine learning

Contact

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