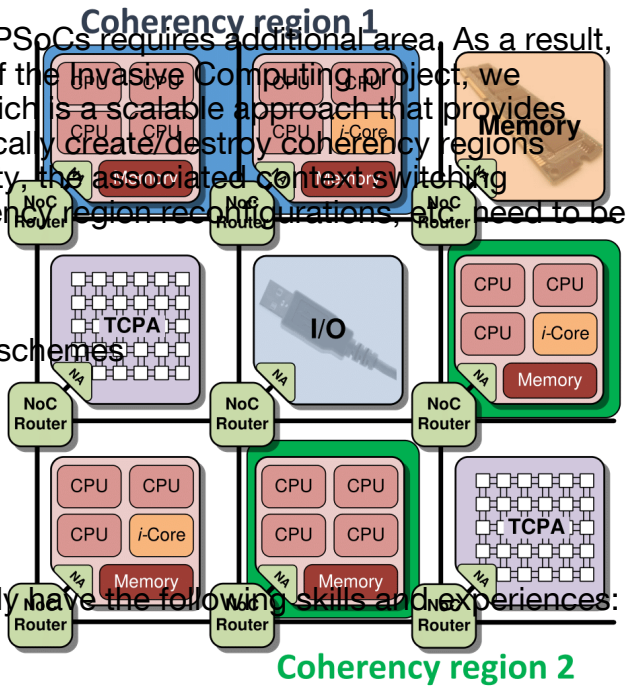
Chair for Integrated Systems
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Forschungspraxis, Master's Thesis

Exploring the Dynamicity of Region Based Cache Coherence for Distributed Shared Memory MPSoCs on an FPGA Prototype

Providing hardware coherence for modern tile-based MPSoCs requires additional area. As a result, this does not scale with increasing tile counts. As part of the Invasive Computing project, we introduced Region Based Cache Coherence (RBCC) which is a scalable approach that provides on-demand coherence. RBCC enables users to dynamically create/destroy coherency regions based on application requirements. With such dynamicity, the associated context switching overheads like cache flushing, directory flushing, coherency region reconfigurations, etc need to be investigated and optimized.



Towards this goal you'll complete the following tasks:
- Investigate existing directory based cache coherence schemes
- Implement/Modify a dynamic framework for RBCC
- Verify the design on a FPGA-based hardware platform

Prerequisites

To successfully complete this project, you should already have the following skills and experiences:
- Very Good VHDL Skills
- Good C/C++ Skills
- Good understanding of MPSoCs and Cache Coherence Schemes
- Self-motivated and structured work style

Contact

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