Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Seminar

Performance Evaluation for RISC-V-based Virtual Prototypes

RISC-V is gaining huge popularity in particular for embedded systems. Recently, a SystemC-based Virtual Prototype (VP) has been open sourced to lay the foundation for providing support for system-level use cases such as design space exploration, analysis of complex HW/SW interactions and power/timing/performance validation for RISC-V based systems. In this work, an efficient core timing model is proposed and integrate it into the VP core to enable fast and accurate performance evaluation for RISC-V based systems.

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