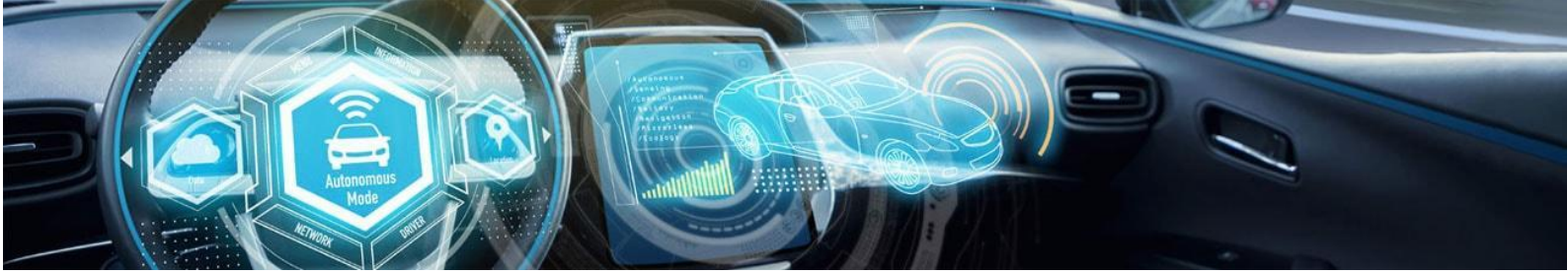

MS Thesis 2 – Automotive SoC Simulation Methodologies for ADAS Software Development Using QEMU and SystemC Simulators: RISC V (ARM ?)

Software development for next generation Automobiles – including Infotainment, advanced driver assistant systems (ADAS) applications – are demanding HW computation performances on-par with the Mobile or Consumer System-on-Chips (SOCs). Similar to the SW development for Mobile SoCs, the automotive SW will require HW Simulators/Emulators at various abstraction levels, in order to perform early SW development in parallel to the HW development (Left shift in HW-SW Co-design).

MS Thesis Objectives

- This MS Thesis project will analyze the requirements for the SoC simulation methodologies for advanced Automotive SoCs from Renesas.
- The Thesis will examine the available HW simulation methods using host-compiled simulators / QEMU and SystemC based models.
- It will cover the benchmarking of trade-offs for performance vs. register accurate SystemC models. Host-compiled models / QEMU are intended to achieve high performance speed with penalty on HW accuracy, while SystemC models intend to achieve high accuracy.
- Methodologies to combine multiple abstraction levels HW simulations, and correspondingly required context switches among these abstraction levels.
- (optionally) Extending the HW simulator/emulator models with supplementary toolchains, E.g. ESESC, Performance estimation toolchain for multicore Emulation on QEMU.

Reference Material

- QEMU vs SystemC, quf2011_02.pdf (upb.de)
- QEMU for performance estimation / ESESC: http://masc.soe.ucsc.edu/docs/hpca13.pdf /
- Context switch for functional simulation

  Daniel Mueller-Gritschneder, Uzair Sharif, Ulf Schlichtmann, **Performance and Accuracy in Soft-Error Resilience Evaluation using the Multi-Level Processor Simulator ETISS-ML**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 2018

Pre-requisites

- Final year of Masters' Study. Study focusses on Microelectronics / EDA / Microprocessors
- Previously completed courses on SoC design technologies / SystemC / High level Synthesis / ML
- Previous experience with C/C++, SystemC, Automotive MPUs
- Optionally, experience with QEMU, SOC simulator methodologies, Machine learning

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