



MS Thesis 1 – Automotive SOC Modeling using Host-Compiled Simulation and Timing Annotation Methods to Recover Software Execution Timings: RISC V (ARM ?)

Software development for next generation Automobiles – including Infotainment, advanced driver assistant systems (ADAS) applications – are demanding HW computation performances on-par with the Mobile or Consumer System-on-Chips (SOCs). Similar to the SW development for Mobile SoCs, the automotive SW will require HW Simulators/Emulators at various abstraction levels, in order to perform early SW development in parallel to the HW development (Left shift in HW-SW Co-design).

MS Thesis Objectives

- This MS Thesis project will analyze the requirements for the SoC simulation methodologies for advanced Automotive SoCs from Renesas.
- The Thesis will examine the available HW simulation methods using Host-Compiled Simulators / QEMU models.
- It will benchmark automotive SW application execution on Host-Compiled Simulators / QEMU.
- Applying existing methods developed by the EDA Lehrstuhl of automated timing annotation using the application data flow graphs (DFGs).
- Benchmarking the annotated timing accuracy compared to SW execution on the Board.
- Methodologies to annotate SW execution timing information to the host-compiled simulation / QEMU.

Reference Material

- QEMU vs SystemC, [quf2011_02.pdf \(upb.de\)](#)
- Kun Lu, Performance Estimation in HW/HW Co-simulation, PhD Thesis, Technische Univesität München, 2015

Pre-requisites

- Final year of Masters' Study. Study focusses on Microelectronics / EDA / Microprocessors
- Previously completed courses on SoC design technologies / SystemC / High level Synthesis / ML
- Previous experience with C/C++, SystemC, Automotive MPUs
- Optionally, experience with QEMU, SOC simulator methodologies, Machine learning

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