

Interdisciplinary Project, Assistant (Student)

## ETISS CoreDSL 2.0 Code Generator

The instruction set simulator [ETISS](#) by TUM EDA uses a generation based approach to create its target CPU simulation models. The models are described in a domain specific language called CoreDSL developed initially by MINRES Technologies GmbH for their ISS project DBT-RISE. The current language specification can be found [here](#).

The original parser for CoreDSL provided by MINRES uses the Eclipse Xtext framework, which was deemed unsuitable for the ETISS project. M2-ISA-R v2 is a tool written in pure python which uses the lark parser library for defining and reading DSLs and mako to generate code from templates.

CoreDSL is in the process of a major revision, and ETISS uses a own dialect with extensions not present in the original specifaion. This project aims at bringing the CoreDSL frontend for M2-ISA-R v2 up to the new CoreDSL specification. Work will be mostly done in Python, with heavy focus on language parsing and processing using the lark library. ETISS is a C++ project and the code generator output is also C++, but not much work will be required in this direction.

### Prerequisites

- Experience using domain specific or formal languages
- Experience with modern C++ and Python
- Ideally previous experience with Eclipse Xtext/Xtend and/or python-lark
- Interest in developing language parsers and processors

### Contact

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### Advisors

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