Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis, Ingenieurspraxis

Semihosting for ETISS instruction set simulator

ETISS is an open source translating instruction set simulator developed at the EDA chair. It is generally usable for all CPU architectures; the focus currently lies on the Open RISC and RISCV architectures.

Semihosting refers to a debugging tool where system calls from the debugging target are intercepted and redirected to the host machine. Useful examples of this include redirection of standard input and output to use text interaction during the development process without having text-capable hardware like serial ports.

ETISS is capable of redirecting console output from the target software to the host environment console. This is currently implemented through special memory locations in the target program code, which has the disadvantage that this memory cannot be mapped otherwise. Sending input to ETISS is also not supported in the current implementation.

Depending on the type of this thesis, the implementation can be more detailed. In case of a combined internship with a bachelor's thesis, a full semihosting system should be implemented.

Tasks:

- Investigate existing console redirection capabilities
- Research existing industry standards and implementations, e.g. for ARM-based CPUs
- Implement basic semihosting capability into ETISS and adapt example program libraries (depending on work type and speed, more functionality can be added)
- Test and benchmark implemented solution to ensure functionality and performance

Prerequisites

- Good C++ experience
- Interest or experience in embedded software development
- Ability to work independently and self-driven
- Ideally experience with semihosting on varios embedded systems

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Advisors

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