Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis

Automatic Translation of Verilog Modules to PyMTL3 Components

Various platforms exist for the developement of Systems on chip (SoCs) and integrated circuits. On one side, classic, commercial tools exist for the design and synthesis flow. Hardware description languages (HDL), like VHDL or Verilog, exist for an efficient modeling and design process. In recent research, also open source solutions in EDA are developed. For example, the PyMTL(3) framework should provide hardware modeling capabilities on various levels of system design [1]. This Python(3)-based framework consists of an own HDL, an API to the elaborated design and the possibility to develop custom extension programs (called Passes) for further investigation. This includes for example already various passes for simulations.

For the developement of new algorithms (e.g. in power modeling [2]), open source benchmark circuits are used for the evaluation. But, many of these circuit designs, as well as available intellectual property (IP) blocks are only available in the dominant HDLs, namely Verilog and VHDL. To take adavantage from the available designs in the PyMTL3 framework, a simple incorporation into the included domain specific language (DSL) is required.

The objective of the thesis would be to develop an automatic Verilog-to-PyMTL3-DSL translator. This includes a familiarization with the PyMTL3 framework and a literature research for applicable IC circuit benchmarks.

[1] Jiang, S., Pan, P., Ou, Y., & Batten, C. (2020). PyMTL3: a Python framework for open-source hardware modeling, generation, simulation, and verification. IEEE Micro, 40(4), 58-66.

[2] Zhou, Y., Ren, H., Zhang, Y., Keller, B., Khailany, B., & Zhang, Z. (2019, June). PRIMAL: power inference using machine learning. In Proceedings of the 56th Annual Design Automation Conference 2019 (pp. 1-6).

Prerequisites

- Experience with Python
- Knowledge in Hardware Description Languages (preferably Verilog, but good knowledge, e.g. in VHDL would be transferable)
- Interest in extending a new open source platform for hardware modeling

Contact

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Advisors

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