

Seminar

# Semihosting in instruction set simulators and virtual platforms

Virtual platforms gain importance in today's semiconductor development as a tool to start software development and verification ahead of the availability of the in-development hardware. Instruction set simulators stand at the core of such virtual platforms, providing a translation layer between the target architecture's machine code and the host system as well as integrating various interfaces to the virtual platform environment. This approach can model entire System-on-Chips purely in software, allowing cross-verification of hardware designs and early software development.

As on real microcontrollers, some means of debugging and user interaction are also required in virtual platforms. Semihosting is an often-used concept which allows the target system to gain access to the host platform's resources, such as standard input/output and filesystem access.

Whereas real hardware usually uses some form of debug probe with host software, in the case of virtual platforms semihosting support needs to be present in the instruction set simulator. Between host and target a protocol is needed which carries the semihosting data.

Finally, the target application also needs to be capable of using the present semihosting channels, usually through a lightweight library.

Tasks:

- Research target-side semihosting implementations for well-known instruction sets
- Research semihosting strategies in simulators
- Compare implementations in ease-of-use, capabilities, etc.

References:

B. Prado, D. Dantas, K. Bispo, T. Fontes, G. Santana and R. Silva, "A Virtual Prototype Semihosting Approach for Early Simulation of Cyber-Physical Systems," 2018 IEEE Symposium on Computers and Communications (ISCC), Natal, 2018, pp. 00208-00213, doi: 10.1109/ISCC.2018.8538621.

S. Werner, L. Masing, F. Lesniak and J. Becker, "Software-in-the-Loop simulation of embedded control applications based on Virtual Platforms," 2015 25th International Conference on Field Programmable Logic and Applications (FPL), London, 2015, pp. 1-8, doi: 10.1109/FPL.2015.7294020.

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