Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Master's Thesis

Generation and development of processor cores for Virtual Prototypes (at Infineon)

Virtual Prototypes (VPs) are generally used in the industry for early software development, verification and testing purposes.

Another important use case is to help in the architecture exploration. For this, it is important to have the ability to use functional models of different processor cores, such as RISC-V, Arm Cortex M0/3 etc. in the VPs. Commercially available SystemC models of processors are usually closed source which comes at the cost of inflexibility of making any enhancements or modifications.

The proposed project aims to overcome the limitations by generating functional processor cores from specifications.

This thesis will be held at Infineon Technologies, their earliest start date is May 1st.

Tasks:

- Surveying the current state-of-the-art, building on existing work on the “ETISS” by academic collaborators at TUM.
- Generation and development of an ARM based processor with ETISS
- Investigation and, if possible, improving the methodology of generation
- Testing and Benchmarking of results using the available reference simulators.

Prerequisites

- Good knowledge of modern C++ and SystemC
- Experience with the ARM Cortex-M profile, ARMv8M architecture and ARM UAL assembly preferred

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